What is claimed is:

1. An integrated circuit memory device comprising:

a memory cell array including a plurality of memory cells;

a bit line sense amplifier configured to amplify data on a pair of bit lines from a memory cell of the memory cell array and to provide the amplified data on a data line and a complementary data line; and

an active load circuit including a first load device electrically connected between the data line and a first voltage source wherein an electrical resistance of the first load device is varied responsive to a voltage level of the data line, and a second load device electrically connected between the complementary data line and the first voltage source wherein an electrical resistance of the second load device is varied responsive to a voltage level of the complementary data line.

2. An integrated circuit memory device according to Claim 1 wherein the electrical resistance of the first load device increases as the voltage level of the data line decreases and wherein the electrical resistance of the second load device increases as the voltage level of the complementary data line decreases.

3. An integrated circuit memory device according to Claim 1 wherein the electrical resistance of the first load device decreases as the voltage level of the data line increases and wherein the electrical resistance of the second load device decreases as the voltage level of the complementary data line increases.

4. An integrated circuit memory device according to Claim 1 wherein the first load device comprises a first load transistor connected between the data line and the first voltage source and wherein the second load device comprises a second load transistor connected between the complementary data line and the first voltage source.

5. An integrated circuit memory device according to Claim 4 wherein the active load circuit further comprises a first control transistor configured to generate a first control signal responsive to the voltage level of the data line and a second control transistor configured to generate a second control signal responsive to the voltage level of the complementary data line with the first control signal being applied to a gate of the first load transistor and with the second control signal being applied to a gate of the second load transistor.

6. An integrated circuit memory device according to Claim 5 wherein the active load circuit further comprises a first diode connected between the complementary data line and the first control transistor and a second diode connected between the data line and the second control transistor.

7. An integrated circuit memory device according to Claim 6 wherein the first and second diodes comprise respective MOS transistors.

8. An integrated circuit memory device according to Claim 4 wherein the first and second load devices comprise respective PMOS transistors.

9. An integrated circuit memory device according to Claim 5 wherein the first control transistor is connected between the gate of the first load transistor and a common node with a gate connected to the data line and wherein the second control transistor is connected between the gate of the second load transistor and the common node with a gate connected to the complementary data line.

10. An integrated circuit memory device according to Claim 9 wherein the first and second control transistors comprise respective first and second NMOS transistors.

11. An integrated circuit memory device according to Claim 9 wherein the active load circuit further comprises an operation control transistor connected between the common node and a second voltage source wherein the operation control transistor is configured to turn on responsive to an activated enable signal and to turn off responsive to a deactivated enable signal.

12. An integrated circuit memory device according to Claim 11 further comprising a precharge device configured to precharge the first and second control signals to the first voltage source responsive to the deactivated enable signal.

13. An integrated circuit memory device according to Claim 12 wherein the precharge device comprises a first precharge transistor connected between the first voltage source and the gate of the first load transistor with a gate receiving the enable signal and a

second precharge transistor connected between the first voltage source and the gate of the second load transistor with a gate receiving the enable signal.

14. An integrated circuit memory device according to Claim 11 wherein the first voltage source comprises a supply voltage and wherein the second voltage source comprises a ground voltage.

15. An integrated circuit memory device according to Claim 1 further comprising:

a current sense amplifier configured to amplify data from the data line and the complementary data line.

16. An integrated circuit memory device according to Claim 1 further comprising:

transmission gates on the pair of complementary data lines configured to couple the bit line sense amplifier to the active load circuit responsive to an enabled selection signal and to decouple the bit line sense amplifier from the active load circuit responsive to a disabled selection signal.

17. A method of operating an integrated circuit memory device including an array of memory cells and a bit line sense amplifier configured to amplify data on a pair of bit lines from a memory cell of the array and to provide the amplified data on a data line and a complementary data line, the method comprising:

varying an electrical resistance between the data line and a voltage source responsive to a voltage level of the data line; and

varying an electrical resistance between the complementary data line and the voltage source responsive to a voltage level of the complementary data line.

18. A method according to Claim 17 wherein varying the electrical resistance between the data line and the voltage source comprises increasing the electrical resistance between the data line and the voltage source as the voltage level of the data line decreases and wherein varying the electrical resistance between the complementary data line and the voltage source comprises increasing the electrical resistance between the complementary data line and the voltage source as the voltage level of the complementary data line decreases.

19. A method according to Claim 17 wherein varying the electrical resistance between the data line and the voltage source comprises decreasing the electrical resistance between the data line and the voltage source as the voltage level of the data line increases and wherein varying the electrical resistance between the complementary data line and the voltage source comprises decreasing the electrical resistance between the complementary data line and the voltage source as the voltage level of the complementary data line increases.

20. A method according to Claim 17 wherein varying the electrical resistance between the data line and the voltage source comprises generating a first control signal responsive to the voltage level of the data line with the electrical resistance between the data line and the voltage source being varied responsive to the first control signal and wherein varying the electrical resistance between the complementary data line and the voltage source comprises generating a second control signal responsive to the voltage level of the complementary data line with the electrical resistance between the complementary data line and the voltage source being varied responsive to the second control signal.

21. A method according to Claim 20 further comprising:

precharging the first and second control signals to a voltage level of the voltage source responsive to a deactivated enable signal.

22. A method according to Claim 17 wherein the voltage source comprises a supply voltage for the memory device.

23. A method according to Claim 17 further comprising:

amplifying data from the data line and the complementary data line.

24. A method according to Claim 17 further comprising:

coupling the bit line sense amplifier to the data line and the complementary data line responsive to an enabled selection signal; and

decoupling the bit line sense amplifier from the data line and the complementary data line responsive to a disabled selection signal.